In response to the Office action, the applicants offer the following remarks.

First, the applicants appreciate the opportunity given their counsel, Mark J. Marcelli, to discuss the subject matter of the claimed invention in a telephonic interview with Examiner Nadav which took place on March 5, 2002. In view of the Examiner interview, the applicants have concluded that an appeal may ultimately be necessary to resolve an existing impasse reach between themselves and the Examiner. Counsel and the Examiner were unable to reach a mutual understanding regarding a specific issue, namely, that it is well-established in the art that self-aligned source and drain structures are distinguishing physical/structural features that provide structural differences and advantages relative to non self-aligned features, and that evidence supplied in the previous Response filed on October 1, 2002, supports the same.

Briefly and in summary, the claimed invention provides an operable field-effect transistor including an amorphous insulative gate dielectric layer having a dielectric constant greater than 5, and self-aligned source/drain regions. The field effect transistor is operable because it includes source and drain regions which have been annealed and activated using a localized, spatially selective annealing process which does not undesirably convert the high-K amorphous dielectric layer to a low-K crystalline layer. The combination of these features is not achievable in the prior art and is not provided by any of the references, taken alone or in combination.

In response to the various paragraphs of the Office action, the applicants offer the following remarks:

I. Claim Rejections Under 35 USC § 112

In the Office action, specifically in paragraph 2, claims 6-8 were rejected under 35 USC § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. The Office action contends that "there is no support for operable self-aligned FET, as recited in claim 6." Applicants respectfully submit that these claim rejections are overcome based on the remarks set forth below.

In the Examiner interview of March 5, 2002, the Examiner's position appeared to be that the embodiment illustrated in Figure 5 represents subsequent processing operations performed on the embodiment shown in Figures 1-3 and that drain extension region 62 was added to the previously illustrated embodiment to render the initially self-aligned source/drain regions now non-self-aligned. Applicants respectfully disagree with this position.

Claim 6 includes the feature of an **operable** self-aligned FET. Applicants respectfully submit that the claimed "operable" FET, including the feature of self-aligned source and drain regions, is enabled by the figures in conjunction with the specification. Figures 1-3 illustrate an FET with self-aligned source and drain regions, that is, source and drain regions that are self-aligned with the gate and include a slight overlap region with the gate. In conjunction with the specification, Figures 2 and 3 also support that the dopants in the self-aligned source and drain regions are activated by the annealing process illustrated in Figures 2 and 3, as required in an "operable" device. The source and drain regions remain self-aligned as shown in Figures 2 and 3. An annealed, activated source/drain area is not structurally distinguished from an unannealed source/drain region in the cross sectional structural views used, and therefore does not require separate illustration to show that the source and drain regions are annealed and the dopants are activated and material defects in the source and drain regions are corrected. The activation by laser annealing is described in the subject specification on page 7, line 10 through page 10, line 9, in conjunction with Figures 1 and 2. Applicants respectfully submit that the combination of figures support the claimed invention because the figures show the self-aligned source and drain region and illustrate and describe that these regions are annealed and activated, as required in an "operable" FET device.

The Office action further states that the "specification recites the initial formation of self-aligned source and drain regions", and also, that the "drawings illustrate that subsequent processing steps result in a final structure whose source and drain regions are not self-aligned with the gate electrode".

Figure 5 is another exemplary embodiment which differs from the exemplary embodiment illustrated in Figures 1-3, and includes drain extension 62. Figure 5 also illustrates another aspect of the invention as it illustrates the substrate in a phase of manufacture subsequent to that shown in Figures 1-3. Applicants respectfully submit that it is clear that:

a) Figure 5, as introduced on page 11, lines 9-15, of the subject specification, is a different embodiment than the one illustrated in Figures 1 - 3. Drain extension 62 is an exemplary additional feature which distinguishes this embodiment and is formed using conventional means. This feature is not included in the embodiment illustrated in Figures 1-3. Figure 5 is included to illustrate that such source and drain extension regions, too, can be annealed by the spatially selective anneal process of the present invention. Just because Figure 5 also illustrates another feature - the subsequently formed vias, does not suggest that Figure 5 is a continuation of the process operations shown in Figures 1-3. Figure 5 does not suggest that the embodiment shown in Figures 1 and 2, has now been further processed such that initially self-aligned source and drain regions have now become non-self-aligned.

Moreover, Applicants respectfully submit that it is inherent and intuitive that if source and drain regions are formed self-aligned with the gate, they remain self-aligned with the gate. The position taken in the Office action is untenable.

b) The embodiment shown in Figures 1-3, as annealed and activated, is an "operable" FET even though illustrated without the vias shown in Figure 5. Applicants respectfully submit that neither of the embodiments are fully completed structures showing wiring and electrical connection and, as such, each are equally "operable" within the definition of the term operable, which is "fit, possible or desirable to use" according to Webster's Third New Unabridged International Dictionary.

As such, the "operable self-aligned FET," as recited in claim 6, is described in the specification in compliance with the requirements of 35 U.S.C. § 112, first paragraph. Claims 7 and 8 depend directly from claim 6. Therefore, the rejection of claims 6-8 under 35 U.S.C. § 112, first paragraph, should be withdrawn.

II. Claim Rejections Under 35 USC § 102

In the Office action, specifically, in paragraph 4, claims 6-7 were rejected under 35 USC § 102(e) as being anticipated by Yu, U.S. Patent 6,194,748, hereinafter "Yu". Applicants respectfully submit that these claim rejections are overcome by the remarks set forth below.

Claim 6 is an independent claim and claim 7 depends directly from claim 6. The Examiner concedes that Yu does not teach source and drain regions being formed self-aligned with the gate structure. The Office action also alleges that "forming source and drain regions self-aligned with the gate structure are processing limitations which do not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced."

Applicants respectfully point out that claim 6 does not recite a step of "forming source and drain regions self-aligned. . . .". Rather, independent claim 6 includes the structural features of a self-aligned source region, and a self-aligned drain region. Such features are structural and not processing limitations as addressed by the Office action. Moreover, Applicants respectfully submit that such features are physical features that are structurally distinguished from non-self-aligned source and drain regions.

Responsive to the Examiner's suggestion in the interview summary, applicants first submit that one of ordinary skill in the art understands a self-aligned source/drain region to be a physical characteristic with structural advantages. Moreover, applicants offer the following evidence to support that a self-aligned region is structurally different from a non-self-aligned region. As discussed during

the Examiner interview, each of the source and drain regions 21 and 22 in Figure 1, are self-aligned with gate 13 even though each include somewhat of an overlap region.

- In Wolf, "Silicon Processing for the VLSI Era", Vol. 1, Lattice Press, on page 318, it states: "Furthermore, the gate itself can serve as a mask during formation of the source and drain regions (by either diffusion or ion implantation)." [*These are self-aligned source and drain regions*]. "The gate thereby becomes nearly perfectly aligned over the channel, with the only overlap of the source and drain being that due to lateral diffusion of the dopant atoms. This *self-alignment* feature simplifies the fabrication sequence, increases packing density, and reduces the gate-source and gate-drain parasitic overlap capacitances."

- U.S. Patent 5,185,278 to Barker, recites (in the Background Section) "Using different mask steps to form the gate electrode, and the source and drain areas often produced transistors that had a misalignment between the gate and the source and drain areas. The misalignment created variations in the gate to drain spacing between transistors which resulted in breakdown voltage variations between transistors".

- Applicants respectfully identify, for the Examiner's information, several U.S. patents that have issued to include self-aligned source and drain regions recited as structural features in device claims. Such patents include U.S. Patent 5,780,892 to Chen, U.S. Patent 5,434,438 to Kuo, U.S. Patent 5,418,393 to Hayden, and U.S. Patent 5,057,898 to Adan, et al.

The above-submitted evidence supports the applicant's previously asserted representation that self-aligned source and drain features are structurally distinguished features as appreciated by one of ordinary skill in the art. These structural features provide physical advantages not achievable by non-self-aligned structures. Moreover, the excerpt from Wolf, indicates that self-aligned source and drain regions include an overlap region when self-aligned with the gate such as appears in the figures. This

provides additional support that the figures and specification support the self-aligned feature, as discussed with respect to the rejections under 35 USC § 112, as above.

Since Yu does not teach or suggest self-aligned source and drain regions as conceded by the Examiner, and since such self-aligned source and drain regions are structurally significant and distinguishing device characteristics recited in claim 6, claim 6 includes features that distinguish the present invention from the cited reference of Yu. Since claim 7 depends from claim 6, then, the rejection of claims 6 and 7 under 35 U.S.C. § 102(e) as being anticipated by Yu, should be withdrawn.

III. Rejection of Claims 6-7 and 9-11 Under 35 USC § 103

In the Office action, specifically in paragraph 6, claims 6-7 and 9-11 were rejected under 35 USC § 103(a) as being unpatentable over Yu in view of admitted prior art (APA) or Shinriki et al. (U.S. Patent 5,292,673), hereinafter "Shinriki". Applicants respectfully submit that these rejections are overcome based on the remarks set forth below.

The proceeding paragraph is offered to provide background information useful in understanding the processing considerations in forming a FET, and points out an advantage of the present invention. Such explanation should not be interpreted, in any way, to limit the scope of the pending device claims.

The art of field effect transistor fabrication teaches that, in order to be operable, the source and drain regions of a transistor must be annealed at an elevated temperature after the source/drain regions are formed. This annealing process utilizes an elevated temperature high enough to activate the dopant impurities, cure the defects associated with introducing impurities into a substrate, and to achieve the desired dopant profile. According to the conventional art for producing a self-aligned source and drain region, and in which the gate structure is used as a mask to form the self-aligned source and drain structures, the self-aligned source/drain regions are necessarily formed after the gate structure, including the gate dielectric and gate electrode, is intact. This means that the annealing process necessary to achieve the desired dopant characteristics, is necessarily carried out after the gate structure including any originally high-K insulative material, is formed using conventional technology. Typical annealing processes are carried out at temperatures of about 800°C-1000° C. Such annealing processes, necessary to produce activated source/drain regions required by an operable field effect transistor, will necessarily convert an amorphous insulative layer, already formed in the transistor gate, to a crystalline or polycrystalline structure and will therefore also lower the dielectric constant of an insulative material which may have been initially formed as a high-K dielectric material. After being exposed to the elevated temperatures typically used for annealing processes,

an originally amorphous, high-K dielectric material will necessarily be converted to a crystalline material having a dielectric constant less than five. As such, according to the prior art, a self-aligned source and drain structure and an amorphous, high-K dielectric, are mutually exclusive in an operable transistor device (i.e., one including annealed source/drain regions). The advantage of the present invention is that the spatially selective annealing process allows for annealing the already formed self-aligned source and drain regions without heating the amorphous high-K dielectric material and converting it to a crystalline film having an undesirably low dielectric constant. This advantage produces the claimed structural advantages of an amorphous high-K insulative layer and self-aligned source and drain regions in a operable field effect transistor, as recited in amended claims 6 and 9.

The Office action states that the cited reference of Yu teaches "an amorphous tantalum pentoxide 34 layer. . . having a dielectric constant greater than 5". While Yu discloses the deposition of an originally-amorphous Ta_2O_5 layer within the gate dielectric structure, Yu does not, however, teach or suggest forming self-aligned source and drain structures in conjunction with this amorphous tantalum pentoxide layer. In fact, Yu clearly indicates that the tantalum pentoxide amorphous layer and the gate itself, are formed *after* high-temperature processes (e.g., greater than 800°C) *are completed* (e.g., silicidation, dopant activation, etc.). [Yu, col. 5, ll. 53-55]. As such, according to Yu, the features of an amorphous tantalum pentoxide gate dielectric layer and self-aligned source and drain regions are mutually exclusive. Yu does not and cannot produce self-aligned source and drain regions because his gates must be formed after the source/drain regions. While the APA and Shinriki each disclose self-aligned source and drain regions, neither makes up for the deficiencies of Yu because neither teaches or suggests self-aligned source and drain regions in conjunction with an amorphous, high-K gate dielectric layer in an operable FET, i.e., an FET having source and drain regions annealed to include activated dopants as in the claimed invention.

It is the **COMBINATION** of the structural features of 1) the self-aligned source and drain regions, 2) the high-K amorphous dielectric layer having a dielectric constant greater than 5, and 3) an operable FET, such as recited in independent claims 6 and 9, that is not achievable in the prior art. It is because of various distinguishing aspects of the present invention, that the above-cited distinguishing structural features are achievable in combination.

Shinriki discloses self-aligned source and drain regions, and a tantalum oxide film included in the gate dielectric. Shinriki does not teach an amorphous insulative layer having a dielectric constant greater than 5. Furthermore, Shinriki discloses high-temperature operations necessarily carried out after the formation of the tantalum oxide film which would necessarily convert the tantalum oxide film

to a crystalline structure. Shinriki discloses an 800°C oxidation process and a 900°C heat treatment following the formation of the tantalum pentoxide. Not only does Shinriki not teach or suggest the feature of an amorphous insulative layer having a dielectric constant greater than 5, the process sequence of Shinriki, in fact, renders it impossible for the tantalum pentoxide to remain a high-k amorphous dielectric layer having a dielectric constant greater than 5.

Although Shinriki, APA, and various other references teach or suggest that self-aligned source and drain features are desirable, according to the prior art, such a feature is not achievable in conjunction with the claimed features of an amorphous insulative layer having a dielectric constant greater than 5 in an operable FET transistor, as recited in claims 6 and 9. None of the cited references, taken alone or in combination, teach or suggest that COMBINATION of features as recited in claims 6 and 9. The Examiner has not upheld the responsibility under 35 USC § 103(a) to show how that of ordinary skill in the art would have been motivated to combine the reference to produce the claimed structure, because it is not possible to combine the cited references to produce the structure including the combination of claimed features.

As such, each of independent claim 6 and 9 include features neither taught nor suggested by the cited references and are therefore distinguished from the references. Claim 7 depends from claim 6 and claims 10 and 11 depend from claim 9 and therefore the rejection of claims 6-7 and 9-11, under 35 USC § 103(a) as being unpatentable over Yu, in view of APA or Shinriki, should be withdrawn.

IV. Rejection of Claim 8 Under 35 USC § 103

In the Office action, specifically in paragraph 7, claim 8 was rejected under 35 USC § 103(a) as being unpatentable over Yu, admitted prior art and Shinriki, as applied to claim 6 above, and further in view of Endo (U.S. Patent 5,596,214), hereinafter "Endo". Applicants respectfully submit that this claim rejection is overcome based on the remarks set forth below.

The cited reference of Endo has apparently been relied upon for disclosing a silicon oxide layer disposed between the insulative layer and the surface region. The cited reference of Endo therefore does not make up for the deficiencies of the references of Yu, APA and Shinriki. Since independent claim 6, the base claim from which dependent claim 8 depends, is distinguished from the references for reasons set forth above, dependent claim 8 is therefore also distinguished from the cited references, taken alone or in combination. Therefore, the rejection of claim 8 under 35 USC § 103(a) as being unpatentable over Yu, APA and Shinriki, in view of Endo, should be withdrawn.

V. Comments Regarding Examiner's Response to Arguments

In the Office action, specifically in paragraphs in 8-10, the Examiner provided commentary responsive to the arguments set forth in Applicants' previous Response of October 1, 2001.

With respect to paragraph 8 of the Office action, applicants respectfully point out that in Yu, the source region and drain regions are features 22 and 24, respectively, while the source extension and drain extension regions are features 23 and 25 respectively, and that it is the source extension and drain extension regions 23 and 25 that are directly aligned with the transistor gate, i.e., directly adjacent gate 36 as in Figure 1 of Yu.

With respect to paragraph 9, applicants offer the following. As recited above and on pages 4-6 of the October 1, 2001 Response, applicants respectfully submit that it is the **COMBINATION** of structural elements of 1) an amorphous high-K gate dielectric having a dielectric constant greater than 5, 2) self-aligned source and drain regions, and 3) an operable transistor (i.e., source/drain regions having dopants activated) that are not achievable and therefore not present in the devices of Yu, APA, Shinriki and Endo. This combination of features is achievable because the present invention provides for selectively annealing and activating the dopant impurities in the annealed regions without significantly heating the amorphous high-K dielectric because of the spatially selective laser anneal aspect of the present invention.

CONCLUSION

For the foregoing reasons, each of claims 6-11 are now in allowable form and the application is therefore in condition for allowance, which action is respectfully requested.

Respectfully submitted,

CHRISTIE, PARKER & HALE, LLP

By _____

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